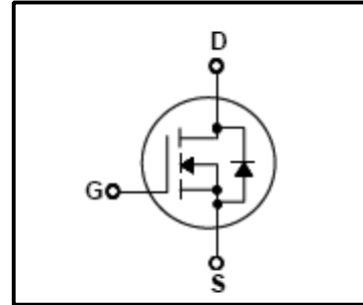


Silicon N-Channel MOSFET

Features

- 70A,60V, RDS(on)(Max0.014Ω)@VGS=10V
- Ultra-low Gate charge(Typical 70nC)
- Low Crss (Typical 160pF)
- Improved dv/dt capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(175°C)



General Description

This Power MOSFET is produced using Semiwell's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a low gate charge with superior switching performance, and rugged avalanche characteristics, DC-DC Converters and power management in portable and battery operated products.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V _{DSS}	Drain Source Voltage	60	V
I _D	Continuous Drain Current(@Tc=25°C)	70	A
	Continuous Drain Current(@Tc=100°C)	51	A
I _{DM}	Drain Current Pulsed (Note1)	280	A
V _{GS}	Gate to Source Voltage	±25	V
E _{AS}	Single Pulsed Avalanche Energy (Note2)	800	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	7.0	V/ ns
P _D	Total Power Dissipation(@Tc=25°C)	158	W
	Derating Factor above 25°C	1.05	W/°C
T _J , T _{stg}	Junction and Storage Temperature	-55~175	°C
T _L	Maximum Lead Temperature for soldering purpose, 1/8 form Case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R _{QJC}	Thermal Resistance , Junction -to -Case	-	-	0.95	°C/W
R _{QCS}	Thermal Resistance , Case-to-Sink	-	0.5	-	°C/W
R _{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	62.5	°C/W

Electrical Characteristics(Tc=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} =±25V,V _{DS} =0V	-	-	±100	nA	
Drain cut -off current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA	
Drain -source breakdown voltage	V _{(BR)DSS}	I _D =250 μA,V _{GS} =0V	60	-	-	V	
Breakdown voltage Temperature Coefficient	ΔBV _{DSS} / ΔT _J	I _D =250μA,Referenced to 25°C	-	0.066	-	V/°C	
Gate threshold voltage	V _{GS(th)}	V _{DS} =10V,I _D =250 μA	2.0	-	4.0	V	
Drain -source ON resistance	R _{DS(ON)}	V _{GS} =10V,I _D =35A	-	-	0.014	Ω	
Input capacitance	C _{iss}	V _{DS} =25V,	-	2350	3050	pF	
Reverse transfer capacitance	C _{rss}	V _{GS} =0V,	-	160	200		
Output capacitance	C _{oss}	f=1MHz	-	690	890		
Switching time	Rise time	tr	V _{DD} =30V, I _D =35A R _G =50Ω (Note4,5)	-	60	130	ns
	Turn-on time	ton		-	30	70	
	Fall time	tf		-	95	200	
	Turn-off time	toff		-	125	260	
Total gate charge(gate-source plus gate-drain)	Qg	V _{DS} =48V, V _{GS} =10V,	-	70	90	nC	
Gate-source charge	Qgs	I _D =70A	-	18	-		
Gate-drain("miller") Charge	Qgd	(Note4,5)	-	24	-		

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	Integral Reverse p-n Junction	-	-	70	A
Pulse drain reverse current	I _{DRP}	Diode in the MOSFET	-	-	280	A
Forward voltage(diode)	V _{DSF}	I _{DR} =70A,V _{GS} =0V	-	-	1.5	V
Reverse recovery time	trr	I _{DR} =70A,V _{GS} =0V,	-	62	-	ns
Reverse recovery charge	Qrr	dI _{DR} / dt =100 A / μs	-	110	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=250uH I_{AS}=70A,V_{DD}=25V,R_G=0Ω, Starting T_J=25°C

3.I_{SD}≤70A,di/dt≤300A/us,V_{DD}<BV_{DSS},STARTING T_J=25°C

4.Pulse Test:Pulse Width≤300us,Duty Cycles≤2%

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

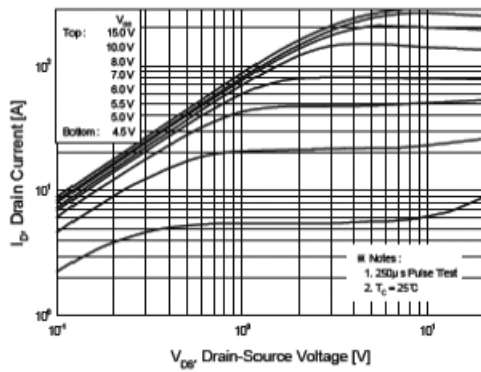


Fig.1 On State Characteristics

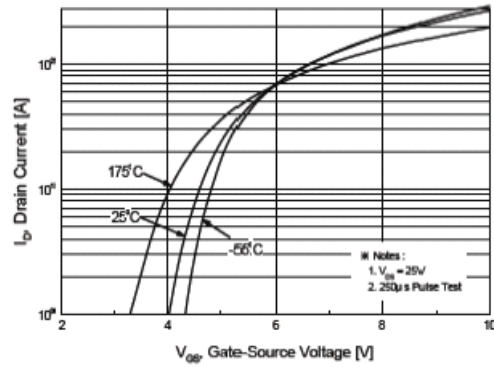


Fig.2 Transfer Characteristics

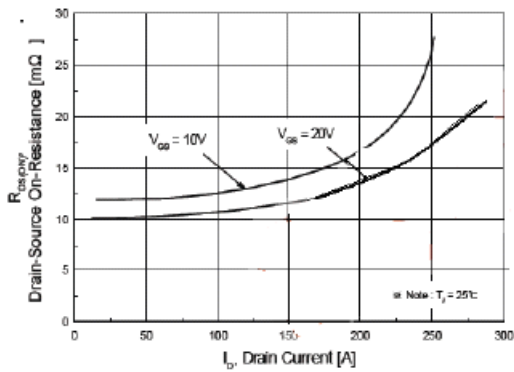


Fig.3 On Resistance Variation Vs Drain Current and Gate Voltage

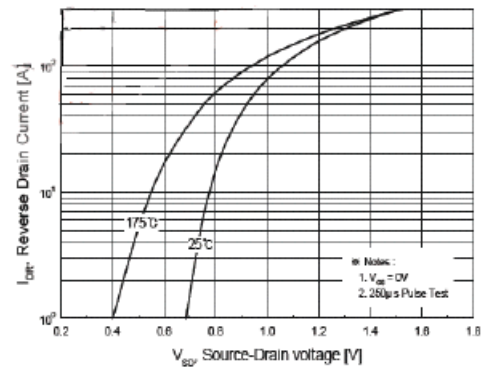


Fig.4 On State Current vs Allowable case Temperature

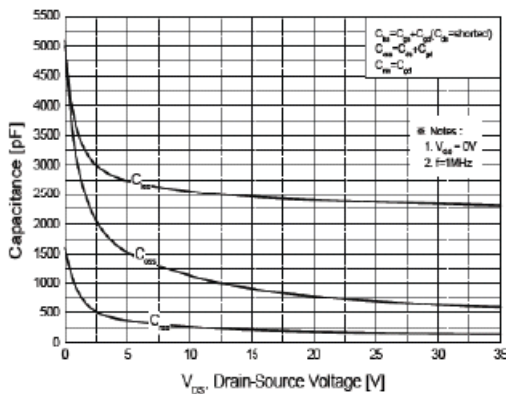


Fig.5 Capacitance Characteristics

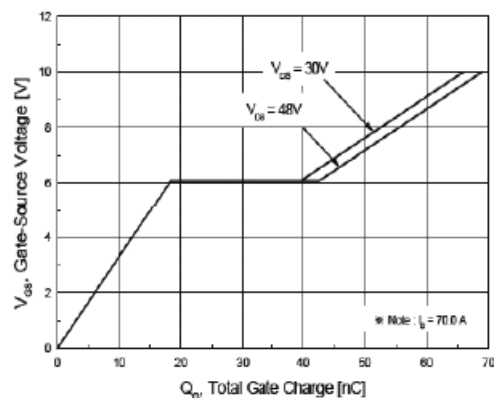


Fig.6 Gate Charge Characteristics

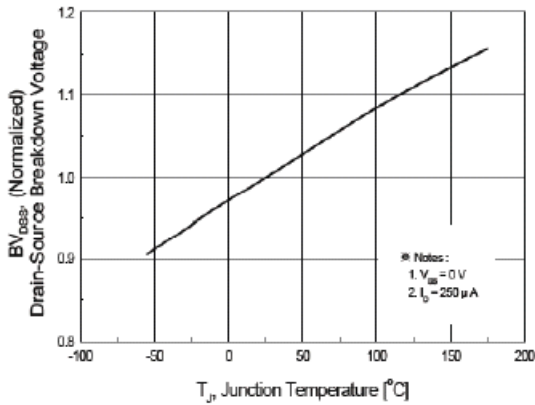


Fig.7 Breakdown Voltage Variation vs. Junction temperature

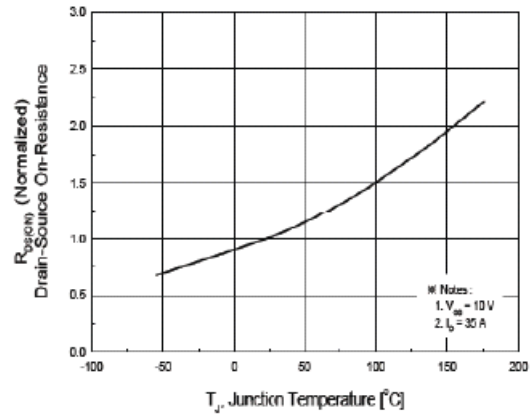


Fig.8 On-Resistance Variation vs. Junction temperature

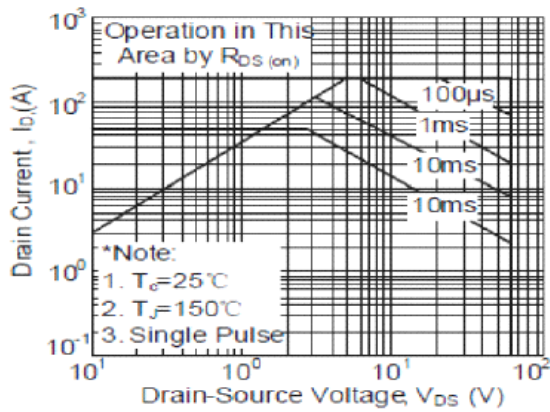


Fig.9 Maximum Safe Operation Area

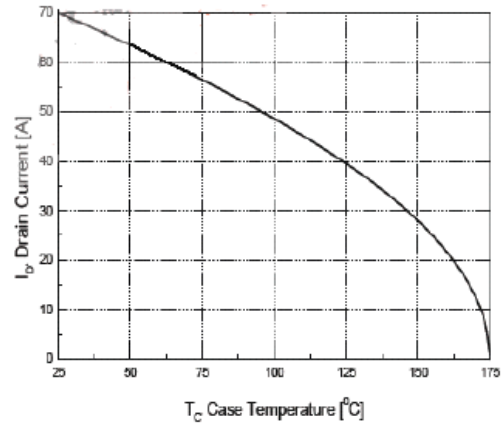


Fig.10 Maximum Drain Current vs. Case temperature

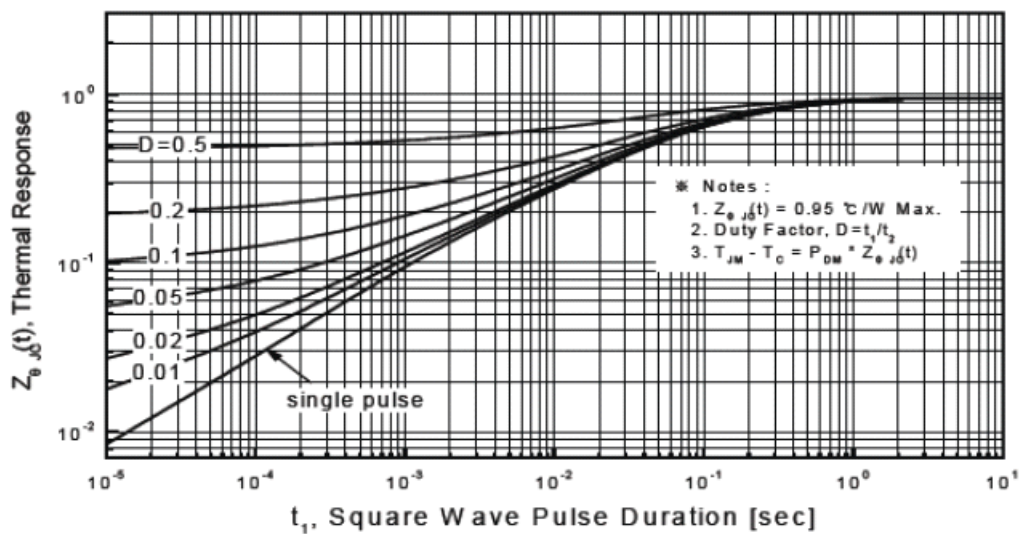


Fig.11 Transient thermal Response Curve

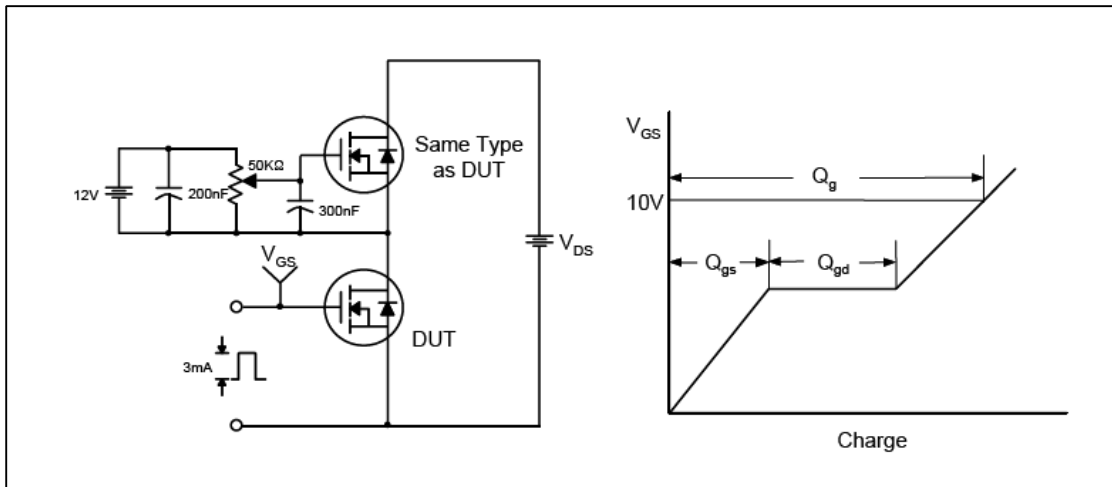


Fig.12 Gate Test circuit & Waveform

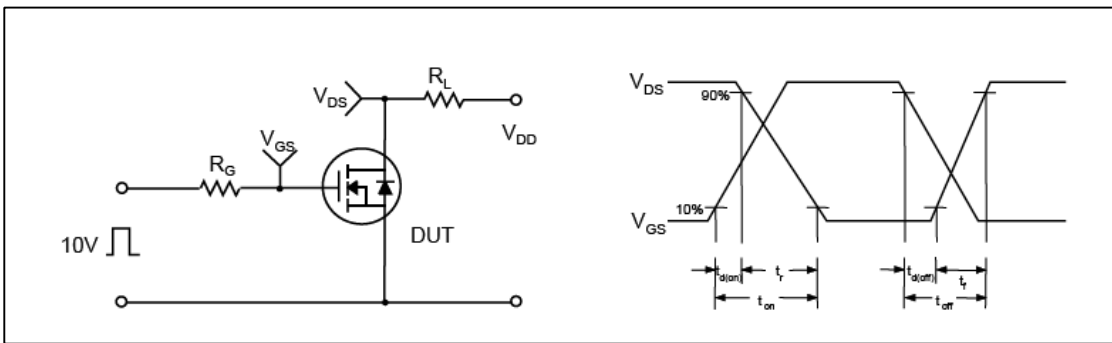


Fig.13 Resistive Switching Test Circuit & Waveform

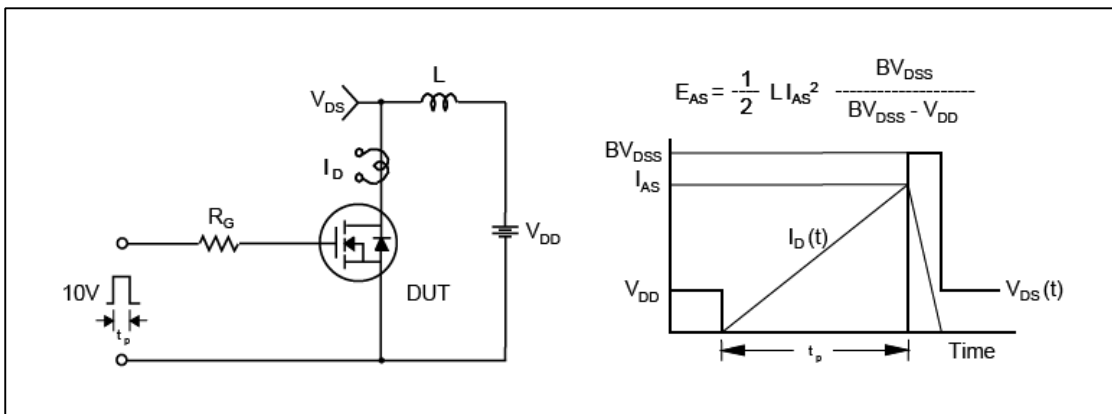


Fig.14 Unclamped Inductive Switching Test Circuit & Waveform

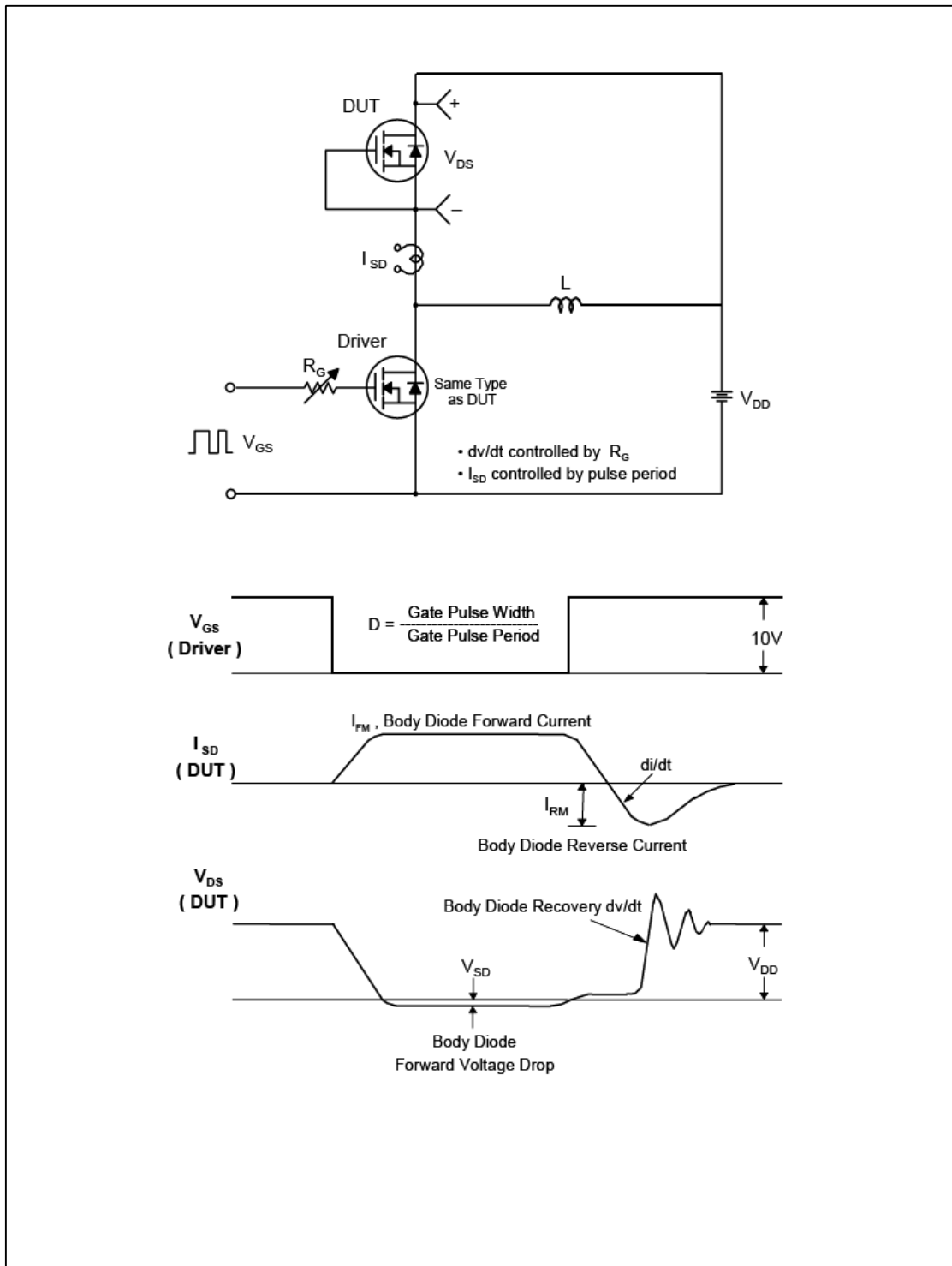


Fig.15 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-220 Package Dimension

