Dual Channel Synchronous Buck PWM Controller for SMPS

Features

- Single 12V Power Supply Required
- Excellent Output Voltage Regulation
  - 1.0V±0.8% Internal Reference Over Line and Temperature
- Simple Single Loop Control Design
  - Voltage Mode PWM Control
- 0~100% Duty Ratio
- Programmable Frequency Range from 50kHz to 400kHz (Constant 50kHz when Floating)
- Integrated Soft-Start and Soft-Off (Patent Pending)
- Support Pre-Biased Power-On
- Both Channel with 180° Phase Shift
- Integrated Boot-Strap Diode
- Over-Current Protection
  - Sense High Side MOSFET's $R_{DS(ON)}$
- 120% Over-Voltage Protection
- 50% Under-Voltage Protection
- Over-Temperature Protection
- Available in SOP-20, TSSOP-20 and TSSOP-20P Packages
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- SMPS

General Description

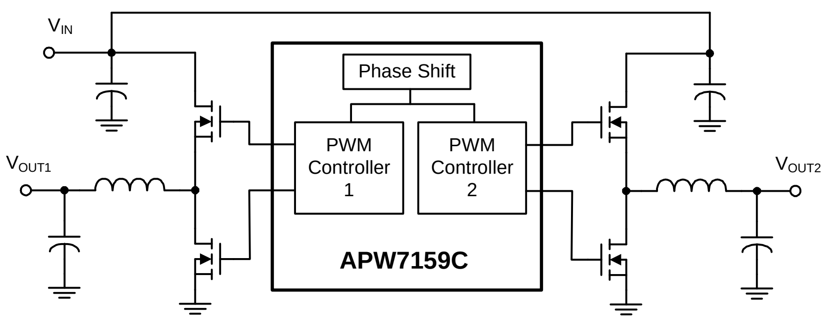
The APW7159C is a dual channel voltage mode and synchronous PWM controller which drives dual N-channel MOSFETs. The two channels are operated with 180 degree phase shift.

The device integrates all of the control, monitoring, and protecting functions into a single package; provides two controlled power output with over-voltage, over-temperature, and over-current protections.

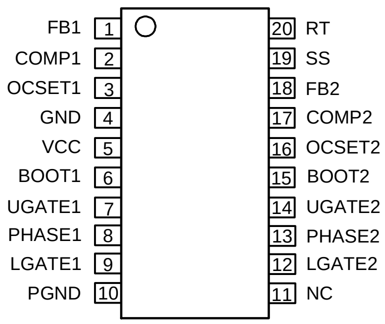
The APW7159C provides excellent regulation for output load variation. The internal 1.0V temperature-compensated reference voltage provides high accuracy of 0.8% over line and temperature. The device includes a 50kHz free-running triangle-wave oscillator that is adjustable from 50kHz to 400kHz.

The APW7159C has been equipped with excellent protection functions: POR, OCP, UVP, and OVP protections. The Power-On-Reset (POR) circuit can monitor the VCC and OCSET voltage to make sure the supply voltage exceeds their threshold voltage while the controller is running. The Over-Current Protection (OCP) monitors the output current by using the voltage drop across the high side MOSFET's $R_{DS(ON)}$. When the output current reaches the trip point, the controller will be latched. Under-Voltage Protection(UVP) and Over-Voltage Protection (OVP) monitor the FB voltage to protect APW7159C from burnout when output voltage is under 50% or over 120% of normal output voltage. The APW7159C is available in SOP-20, TSSOP-20 and TSSOP-20P packages.

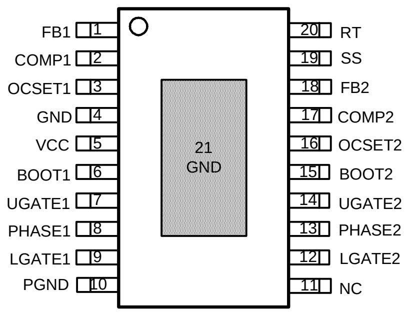
Simplified Application Circuit



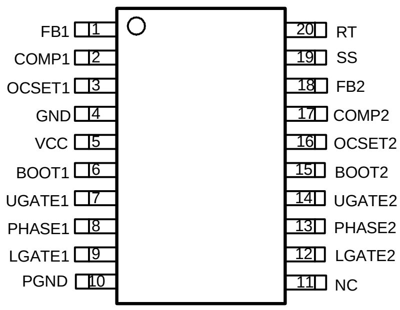
Pin Configuration



SOP-20
(Top view)



TSSOP-20P
(Top view)



TSSOP-20
(Top view)

Ordering and Marking Information

APW7159C □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-20 R : TSSOP-20P O : TSSOP-20 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7159C K: 	XXXXX - Date Code
APW7159C R/O: 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter		Rating	Unit
V_{VCC}	Input Bias Supply Voltage (VCC to GND)		-0.3 ~ 16	V
$V_{BOOT1/2}$	BOOT1/ BOOT2 to PHASE1/PHASE2 Voltage		-0.3 ~ 16	V
	UGATE1/UGATE2 to PHASE1/PHASE2	<400ns pulse width	-5 ~ $V_{BOOT1/2}$+5	V
		>400ns pulse width	-0.3 ~ $V_{BOOT1/2}$+0.3	V
	LGATE1/LGATE2 to PGND Voltage	<400ns pulse width	-5 ~ V_{VCC}+0.3	V
		>400ns pulse width	-0.3 ~ V_{VCC}+0.3	V
	PHASE1/PHASE2 to PGND Voltage	<400ns pulse width	-10 ~ 30	V
		>400ns pulse width	-0.3 ~ 16	V
	RT, SS, COMP1, COMP2, FB1, FB2 to GND Voltage		-0.3 ~ 7	V
	OCSET1, OCSET2 to GND		-0.3 ~ V_{VCC}+0.3	V
	PGND to GND Voltage		-0.3 ~ 0.3	V
P_D	Power Dissipation T_A=25°C SOP-20 TSSOP-20P TSSOP-20		1 2.2 1.1	W
	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note 1 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air (Note 2) SOP-20 TSSOP-20P TSSOP-20	100 45 92	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance SOP-20 TSSOP-20P TSSOP-20	12 4 20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VCC}	Input Bias Supply Voltage (VCC to GND)	10 ~ 13.2	V
V_{IN1}/V_{IN2}	Converter Input Voltage	2 ~ 13.2	V
V_{OUT1}/V_{OUT2}	Converter Output Voltage	1 ~ V_{IN1}/V_{IN2}	V
I_{OUT1}/I_{OUT2}	Converter Output Current	0 ~ 30	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{OUT}= 3.3V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7159C			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VCC Supply Current (Shutdown Mode)	V_{VCC}<5V, SS=GND	-	1	2	mA
I_{VCC}	VCC Supply Current	UGATE1/UGATE2 and LGATE1/LGATE2 open	-	5	10	mA
POWER-ON-RESET (POR) AND LOCKOUT VOLTAGE THRESHOLDS						
	Rising VCC Threshold		9	9.5	10	V
	Falling VCC Threshold		-	4.6	-	V
	Rising V_{OCSET1}/V_{OCSET2} Threshold		-	1.6	-	V
	Falling V_{OCSET1}/V_{OCSET2} Threshold		-	1.0	-	V
OSCILLATOR						
F_{OSC}	Free Running Frequency	R_T = NC, V_{VCC} =12V	45	50	55	kHz
	Programmable Frequency Range	Connect Resistor from RT to GND	45	-	400	kHz
	Total Frequency Accuracy	Over-Temperature	-10	-	10	%
V_{OSC}	Ramp Amplitude (Note 4)		-	1.9	-	V
	Duty Cycle		0	-	100	%
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	1.0	-	V
	Reference Voltage Tolerance	V_{VCC}=10V~13.2V	-0.8	-	+0.8	%
	Load Regulation (Note 4)	I_{OUT1}= I_{OUT2}=0A~10A	-	0.01	-	%/A
PWM ERROR AMPLIFIERS						
	Open Loop Gain (Note 4)	R_L=10kΩ, C_L=10pF (Note 4)	-	88	-	dB
	Unity-Gain Bandwidth (Note 4)	R_L=10kΩ, C_L=10pF (Note 4)	-	15	-	MHz
	Slew Rate (Note 4)	R_L=10kΩ, C_L=10pF (Note 4)	-	6	-	V/μs
	FB1/FB2 Input Current	V_{FB1}/V_{FB2}=1.0V	-	-	0.1	μA
	COMP1/COMP2 Source Current	V_{COMP}=2V	-	5	-	mA
	COMP1/COMP2 Sink Current	V_{COMP}=2V	-	5	-	mA
BOOT-STRAP DIODE AND SOFT-START						
V_F	Diode Forward Voltage	I_F=10mA	-	0.8	-	V
I_{SS}	Soft-Start Charge Current		24	30	36	μA

Electrical Characteristics (Cont.)

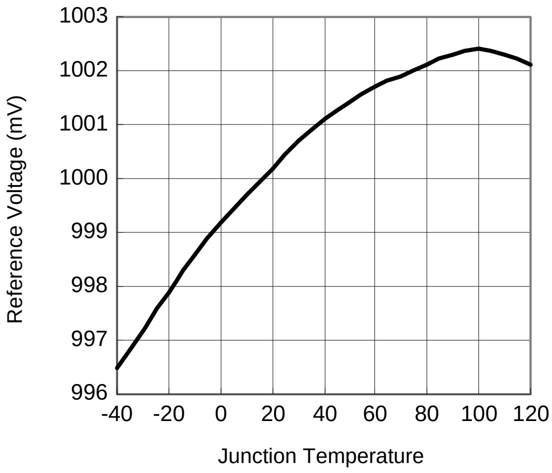
Unless otherwise specified, these specifications apply over V_{IN}=12V, V_{OUT}= 3.3V and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7159C			Unit
			Min.	Typ.	Max.	
GATE DRIVERS						
I_{UGATE1}/ I_{UGATE2}	High Side Gate Source Current	V_{BOOT1}=V_{BOOT2}=12V, V_{UGATE1}-V_{PHASE1}= 2V /V_{UGATE2} – V_{PHASE2}=2V	-	1.7	-	A
	High Side Gate Sink Current	V_{BOOT1}=V_{BOOT2}=12V, V_{UGATE1}-V_{PHASE1}= 10V /V_{UGATE2} – V_{PHASE2}=10V	-	1.1	-	A
I_{LGATE1}/ I_{LGATE2}	Low Side Gate Source Current	V_{VCC}=12V, V_{LGATE1}=V_{LGATE2}=2V	-	1.9	-	A
	Low Side Gate Sink Current	V_{VCC}=12V,V_{LGATE1}= V_{LGATE2}=10V	-	1.6	-	A
	Dead Time 1 (Note 4)	UGATE1/UGATE2 Falling to LGATE1/LGATE2 Rising	-	40	-	ns
	Dead Time 2 (Note 4)	LGATE1/LGATE2 Falling to UGATE1/UGATE2 Rising	-	40	-	ns
PROTECTION						
I_{OCSET1}/ I_{OCSET2}	OCSET1/OCSET2 Current Source		180	200	220	μA
	Over Voltage Protection	Measure on FB1/FB2	115	120	125	%V_{REF}
	Under Voltage Protection	Measure on FB1/FB2	45	50	55	%V_{REF}
	Over-Temperature Shutdown (Note 4)		-	150	-	°C
	Over-Temperature Hysteresis (Note 4)		-	40	-	°C

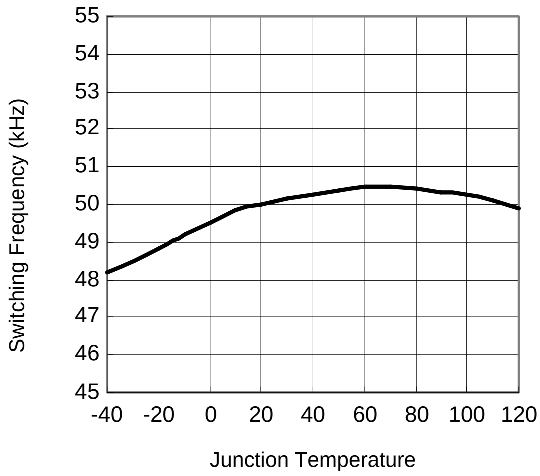
Note 4: Guarantee by design, not production test

Typical Operating Characteristics

Reference Voltage vs. Junction Temperature



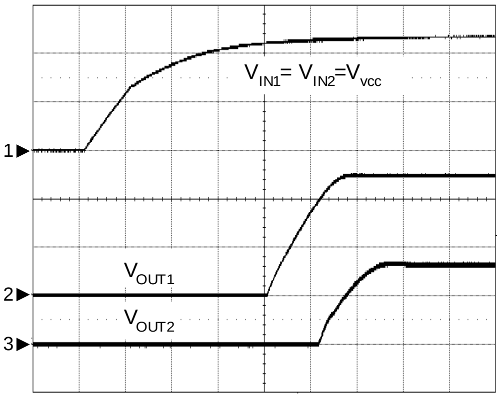
Switching Frequency vs. Junction Temperature



Operating Waveforms

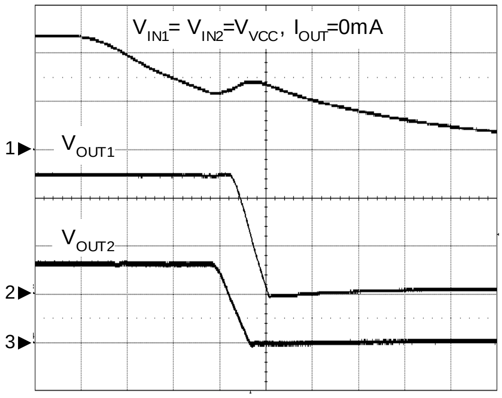
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Power On



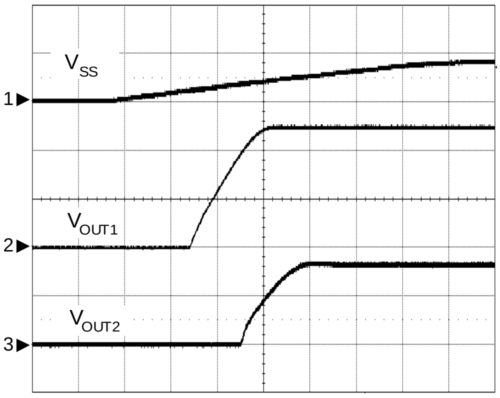
CH1: V_{IN1}=V_{IN2}=V_{VCC}, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{OUT2}, 2V/Div
Time: 2ms/Div

Power Off



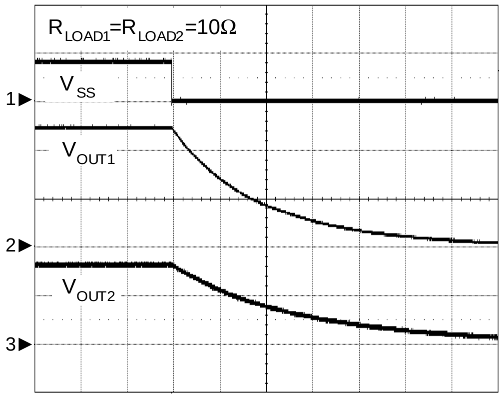
CH1: V_{IN1}=V_{IN2}=V_{VCC}, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{OUT2}, 2V/Div
Time: 5ms/Div

Enable



CH1: V_{SS}, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{OUT2}, 2V/Div
Time: 2ms/Div

Shutdown

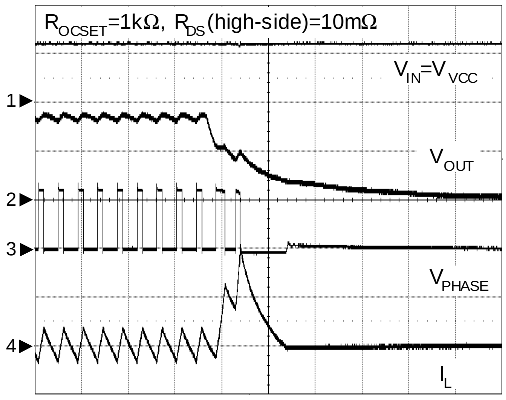


CH1: V_{SS}, 5V/Div
CH2: V_{OUT1}, 2V/Div
CH3: V_{OUT2}, 2V/Div
Time: 10ms/Div

Operating Waveforms (Cont.)

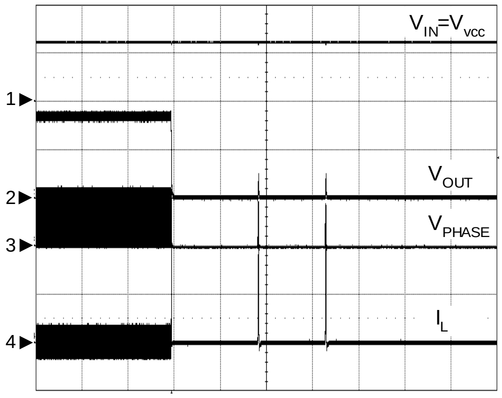
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Short-Circuit Protection



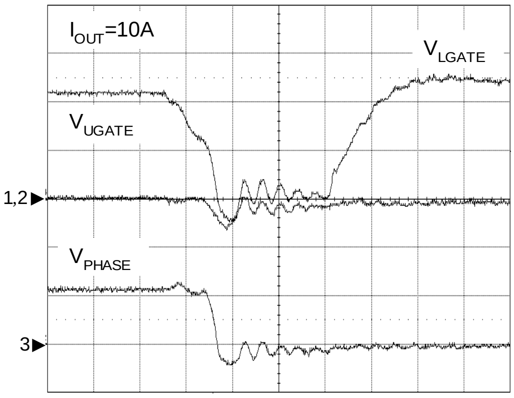
CH1: V_{IN}=V_{VCC}, 10V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{PHASE}, 10V/Div
CH4: I_L, 10A/Div
Time: 50μA/Div

Over-Current Protection



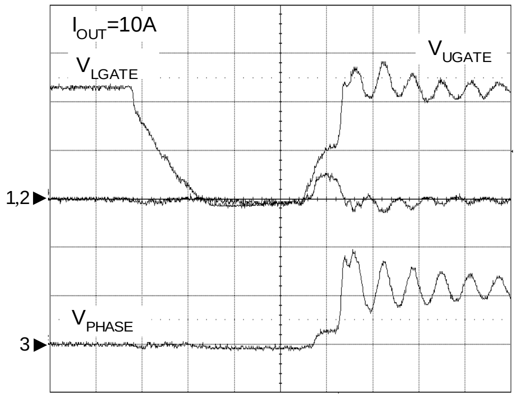
CH1: V_{IN}=V_{VCC}, 10V/Div
CH2: V_{OUT}, 2V/Div
CH3: V_{PHASE}, 10V/Div
CH4: I_L, 10A/Div
Time: 10ms/Div

UGATE Falling



CH1: V_{UGATE}, 10V/Div
CH2: V_{LGATE}, 5V/Div
CH3: V_{PHASE}, 10V/Div
Time: 20ns/Div

UGATE Rising

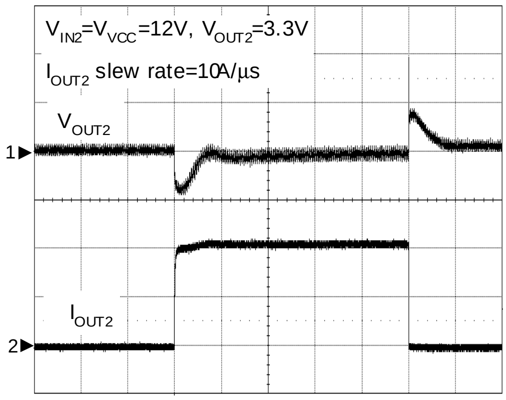


CH1: V_{UGATE}, 10V/Div
CH2: V_{LGATE}, 5V/Div
CH3: V_{PHASE}, 10V/Div
Time: 20ns/Div

Operating Waveforms (Cont.)

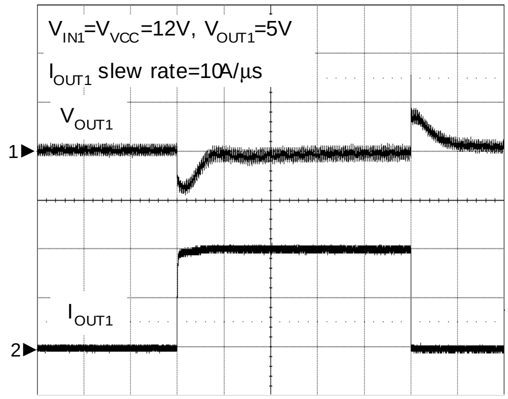
Refer to the typical application circuit. The test condition is V_{IN}=12V, T_A= 25°C unless otherwise specified.

Load Transient Response



CH1: V_{OUT2}, 200mV/Div
CH2: I_{OUT2}, 5A/Div
Time: 100µs/Div

Load Transient Response



CH1: V_{OUT1}, 200mV/Div
CH2: I_{OUT1}, 5A/Div
Time: 100µs/Div

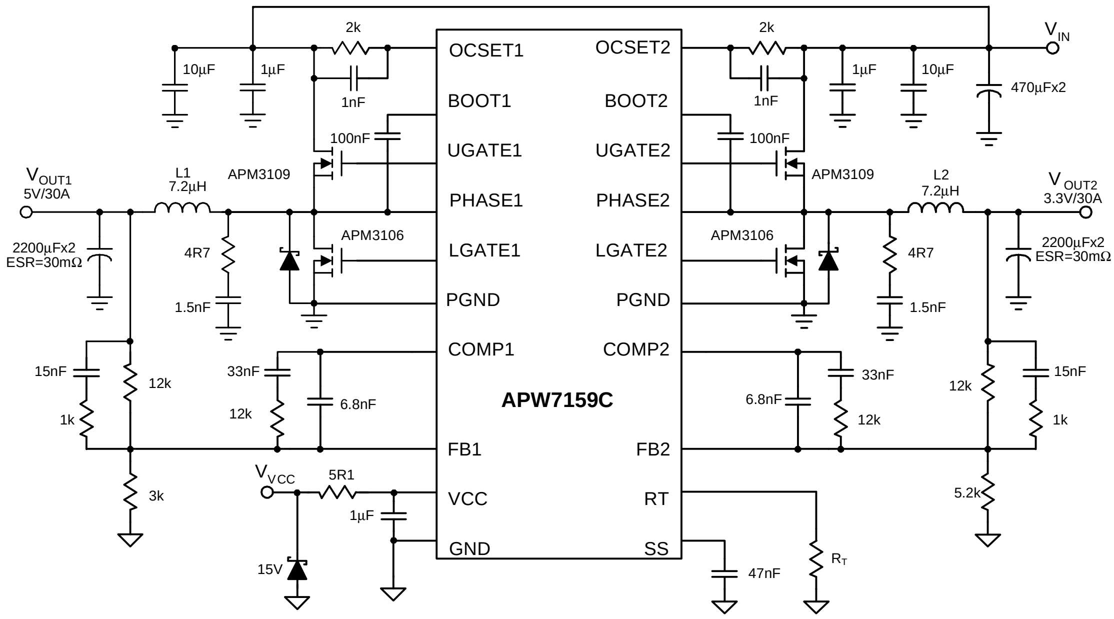
Pin Description

PIN			FUNCTION
NO.		NAME	
SOP-20/ TSSOP-20	TSSOP-20P		
1	1	FB1	Feedback Input of Channel 1. The Buck converter senses feedback voltage via FB1 and regulates the FB1 voltage at 1.0V. Connecting FB1 with a resistor-divider from the output sets the output voltage of the Buck converter.
2	2	COMP1	Error Amplifier Output of Channel 1. It is used to compensate the regulation control loop. Refer to the section “Application Information” for details.
3	3	OCSET1	This pin is used to set the maximum inductor current of channel 1. Refer to the section in “Function Description” for detail.
4	4	GND	Signal Ground.
5	5	VCC	Power Supply Input. Connect a nominal 10V to 13.2V power supply voltage to this pin. A power-on-reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10µF) should be connected to the GND for noise decoupling.
6	6	BOOT1	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE1 to BOOT1, an internal diode, and the power supply voltage VCC, generate the bootstrap voltage for the high-side gate driver (UGATE1).
7	7	UGATE1	High-Side Gate Driver Output of Channel 1. This pin is the gate driver for high-side MOSFET.
8	8	PHASE1	This pin is the return path for the high-side gate driver 1. Connect this pin to the high-side MOSFET source and connect a capacitor to BOOT1 for the bootstrap voltage. This pin is also used to monitor the voltage drop across the MOSFET for over-current protection.

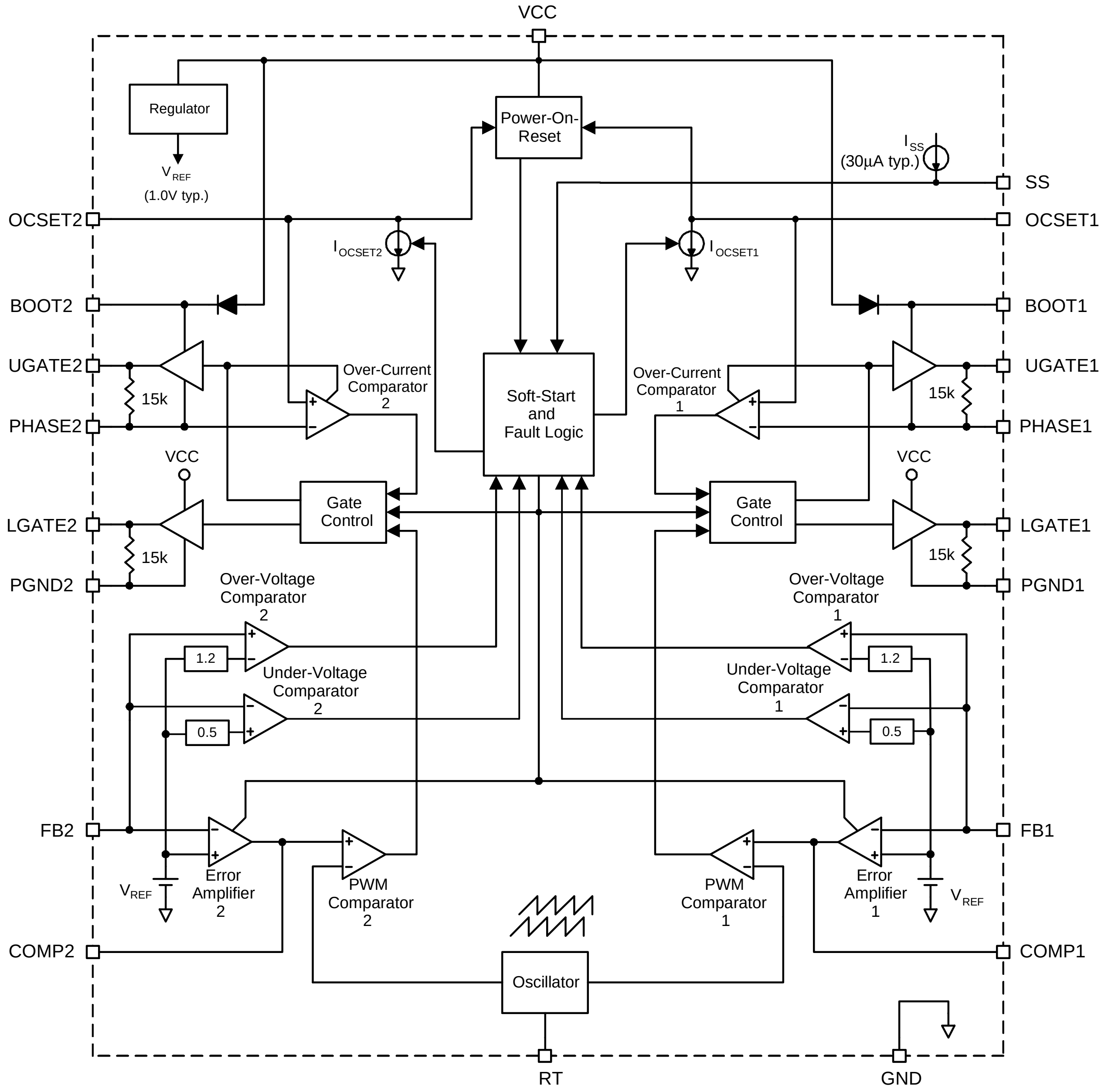
Pin Description (Cont.)

PIN			FUNCTION
NO.		NAME	
SOP-20/ TSSOP-20	TSSOP-20P		
9	9	LGATE1	Low-side Gate Driver Output of channel 1. This pin is connected to low-side MOSFET.
10	10	PGND	Power Ground of the Low-Side Gate Drivers. Use a separate track to connect this pin to Source of the low-side MOSFET. The Source of the low-side MOSFET must be connected to system ground with very low impedance. Connecting this pin to the GND.
11	11	NC	No Connection.
12	12	LGATE2	Low-side Gate Driver Output of channel 2. This pin is the gate driver for low-side MOSFET.
13	13	PHASE2	This pin is the return path for the high-side gate driver of channel 2. Connect this pin to the high-side MOSFET source and connect a capacitor to BOOT2 for the bootstrap voltage. This pin is also used to monitor the voltage drop across the MOSFET for over-current protection.
14	14	UGATE2	High-side Gate Driver Output of Channel 2. This pin is connected to high-side MOSFET.
15	15	BOOT2	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE2 to BOOT2, an internal diode, and the power supply voltage VCC, generate the bootstrap voltage for the high-side gate driver (UGATE2).
16	16	OCSET2	This pin is used to set the maximum inductor current of channel 2. Refer to the section in “Function Description” for detail.
17	17	COMP2	Error Amplifier Output of Channel 2. It is used to compensate the regulation control loop. Refer to the section “Application Information” for details.
18	18	FB2	Feedback Input of Channel 2. The converter senses feedback voltage via FB2 and regulates the FB2 voltage at 1.0V. Connecting FB2 with a resistor-divider from the output sets the output voltage of the Buck converter.
19	19	SS	Connect a capacitor to the GND and a 30μA current source charges this capacitor to set the soft-start time. The pin also integrates EN/Shutdown function. Pulling SS below 0.7V shuts down the IC.
20	20	RT	This pin allows adjusting the switching frequency. Connect a resistor from RT to the ground to increase the switching frequency.
-	21	Exposed Pad	Connect the pad to the system ground plane on PCBs. The PCB will be a heat sink of the IC.

Typical Application Circuit



Block Diagram



Function Description

VCC Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7159C continually monitors the voltage on VCC and OCSET1/OCSET2 pin. When the voltage on VCC and OCSET1/OCSET2 exceeds their rising POR threshold voltage respectively (9.5V and 1.6V typical), the POR function initiates soft-start operation. Where the voltage at OCSET1/OCSET2 pin is equal to V_{IN1}/V_{IN2} minus a fixed voltage drop ($V_{OCSET1}/V_{OCSET2} = V_{IN1}/V_{IN2} - V_{ROCSET1}/V_{ROCSET2}$). For operation with a single +12V power source, V_{IN1}/V_{IN2} and VCC are equivalent and the +12V power source must exceed the rising VCC threshold. With all input supplies above their POR thresholds, the device initiates a soft-start interval.

Soft-Start

The SS pin controls the soft-start and enables/disables the controller. Connect a soft-start capacitor from SS pin to GND to set the soft-start interval. Figure1 shows the soft-start interval. When VCC reaches its Power-On-Reset threshold (9.5V typical), a soft-start current source, I_{SS} (30µA typical), starts to charge the capacitor. When the V_{SS} reaches the threshold about 1V, the internal 1.0V reference starts to rise and follows the V_{SS}; the error amplifier output (V_{COMP}) suddenly rises to 1.1V, which is the valley of the triangle wave of the oscillator, leads the V_{OUT1}/V_{OUT2} to start up. V_{OUT1} and V_{OUT2} have power on sequence issue, V_{OUT2} will start up after V_{SS} rise up to 1.4V. The soft-start time can be calculated as below:

$$T_{SOFT-START} = t_3 - t_1 = t_4 - t_2 = \frac{C_{SS}}{I_{SS}} \cdot 1V$$

Where

C_{SS} = external capacitor connected at SS pin

I_{SS} = soft-start current, typical I_{SS} current is 30µA

The APW7159C does not have EN pin, pull SS low (SS <0.7V) shut down the IC.

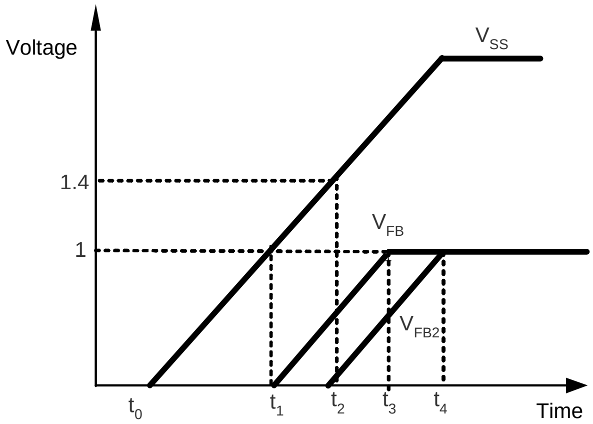


Figure 1. Soft start timing sequence

Soft-Off (5V<VCC<9V) (Note 5)

The APW7159C also integrates a soft-off circuitry. When the voltage on VCC falls below the falling threshold1 (8V typical), an internal current source, I_{SS} (30µA typical), starts to discharge from SS. When the V_{VCC} falls below the falling threshold2 (4.6V typical), the device is shutdown. The APW7159C will initiate a soft-start process until re-cycle power supply (9.5V typical).

Note 5: The mentioned soft-off function is patent pending by ANPEC

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7159C. When the junction temperature exceeds 150°C, a thermal sensor pulls UGTAE1/UGATE2 and LGATE1/LGATE2 low, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and to regulate the output voltage again after the junction temperature cools by 40°C. The OTP is designed with a 40°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the lifetime of the device.

Over-Current Protection

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage, which the product of the inductor's current and high side MOSFET on-resistance during it's on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

Function Description (Cont.)

Over-Current Protection (Cont.)

A resistor (R_{OCSET1}/R_{OCSET2}) connected between OCSET1/OCSET2 pin and the drain of the upper MOSFET will determine the over-current limit. An internal current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the upper MOSFET. When the voltage across the upper MOSFET exceeds the voltage drop across the R_{OCSET1}/R_{OCSET2}, the IC shuts off the entire gate drives. After a soft-start period delay, the APW7159C initiates a new soft-start process. After 3 times over-current events are counted continuously, all devices and gate drivers (UGATE1/UGATE2/LGATE1/LGATE2) were shutdown. Both outputs of the PWM converter are latched to be floating. The threshold of the over-current limit is therefore given by :

$$I_{LIMIT} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(ON)}(high - side)}$$

For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be determined.

- The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.

-The minimum I_{OCSET1}/I_{OCSET2} (typical 200μA) and minimum R_{OCSET1}/R_{OCSET2} should be used in the above equation.

-Note that the I_{LIMIT} is the current flow through the upper MOSFET; I_{LIMIT} must be greater than maximum output current add the half of inductor ripple current.

The over-current protection will shut down the device and discharge the C_{SS} with a 30μA sink current. If the R_{OCSET1}/R_{OCSET2} is not connected or V_{OCSET1}/V_{OCSET2} is below 1.6V, the APW7159C will not initiate soft-start process and force device shutdown.

Under-Voltage Protection

The under-voltage function monitors the voltage on FB by Under-Voltage comparator to protect the PWM converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold (50% V_{REF}), a fault signal is internally generated and the device turns off high-side and low-side MOSFETs. The converter is shutdown and the output is latched to be floating.

Over-Voltage Protection

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage. When the output voltage rises to 120% of the nominal output voltage, the APW7159C turns off all devices. The APW7159C will initiate a soft-start process until re-cycle power supply.

Adaptive Shoot-Through Protection

The gate driver incorporates adaptive shoot-through protection to high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the low-side MOSFET, the LGATE1/LGATE2 voltage is monitored until it reaches a 1.6V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side MOSFET, the UGATE1/UGATE2 to PHASE1/PHASE2 voltage is also monitored until it reaches a 1.6V threshold, at which time the LGATE1/LGATE2 is released to rise after a constant delay.

Pre-Bias Power-On

When the APW7159C initiates the soft-start, the output voltage will smoothly rising without discharged even the voltage is not zero.

Switching Frequency

The APW7159C provides the oscillator switching frequency adjustment. The device includes a 50kHz free-running triangle wave oscillator. If operates in higher frequency than 50kHz, connect a resistor from RT pin to the ground to increase the switching frequency. Equation 1 and figure 2 shows the relationship between oscillation frequency and RT resistance.

$$F_{OSC}(kHz) = 50 + \frac{7550}{R_T(k\Omega)}$$

Function Description (Cont.)

Switching Frequency (Cont.)

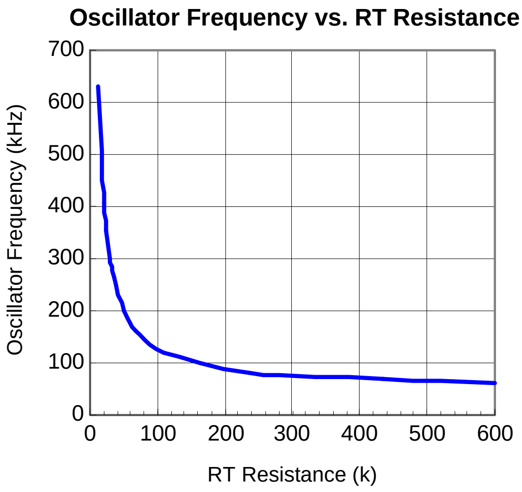


Figure 2. Oscillator Frequency vs. RT Resistance

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 1V. The output voltage is determined by:

$$V_{OUT} = 1 \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Where R_{OUT} is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to the GND.

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where Fs is the switching frequency of the regulator.

Although increase of the inductor value and frequency reduces the ripple current and voltage, a tradeoff will exist between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_S) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be parallelled to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The RMS current of the bulk input capacitor is calculated as the following equation:

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)}$$

During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1μF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. There are two components of loss in the MOSFETs: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{OUT}^{\ 2}(1 + TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$$

$$P_{LOWER} = I_{OUT}^{\ 2}(1 + TC)(R_{DS(ON)})(1\text{-}D)$$

Where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Application Information (Cont.)

MOSFET Selection (Cont.)

Note that both MOSFETs have conduction loss while the upper MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 6. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

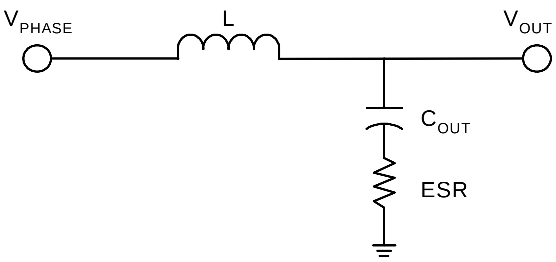


Figure 3. The Output LC Filter

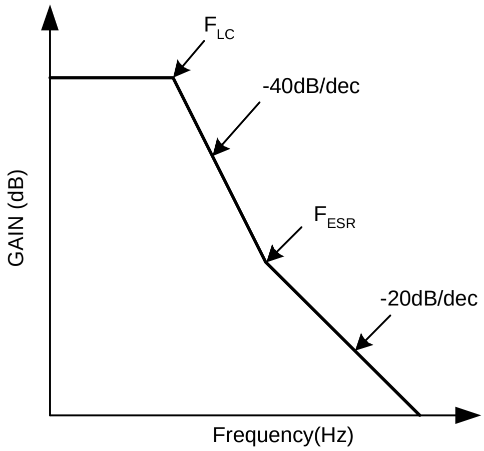


Figure 4. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 5. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

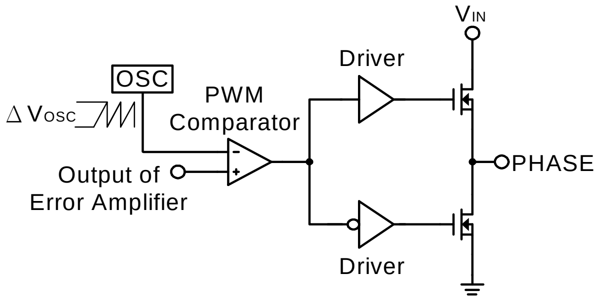


Figure 5. The PWM Modulator

The compensation network is shown in Figure 6. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

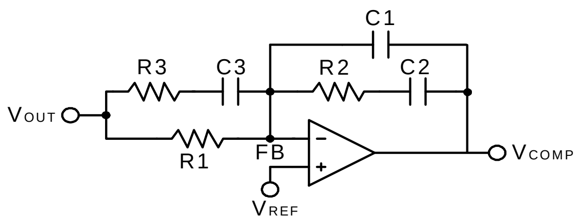


Figure 6. Compensation Network

Application Information (Cont.)

PWM Compensation (Cont.)

The closed loop gain of the converter can be written as:

$GAIN_{LC}$ X $GAIN_{PWM}$ X $GAIN_{AMP}$

Figure 7. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similars to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency

F_O: (1/5 ~ 1/10) X $F_S > F_O > F_{ESR}$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

F_{Z1} = 0.75 X F_{LC}

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

$F_{P1} = F_{ESR}$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5 X F_S

$F_{Z2} = F_{LC}$

Combine the two equations will get the following component calculations:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

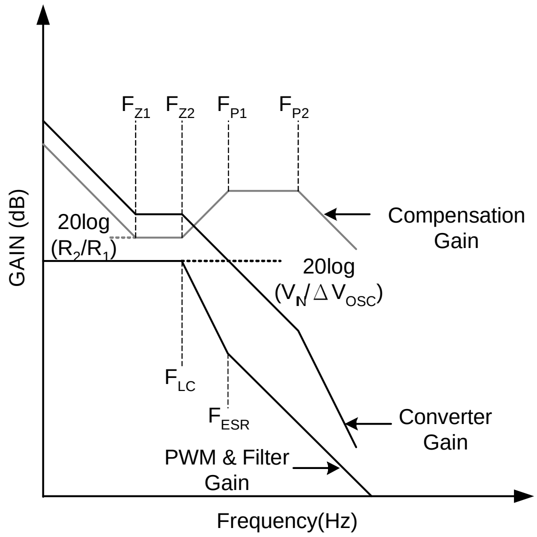


Figure 7. Converter Gain and Frequency

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 200kHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating till combined using the ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines

Application Information (Cont.)

Layout Consideration (Cont.)

indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the lower MOSFET GND.
- The drain of the MOSFETs (VIN and PHASE nodes) should be a large plane for heat sinking.
- The R_{OCSET} resistance should be placed near the IC as close as possible.
- The decoupling capacitor for VCC should be placed near the VCC and GND. C_{BOOT} should be connected as close to the BOOT and PHASE pins as possible.

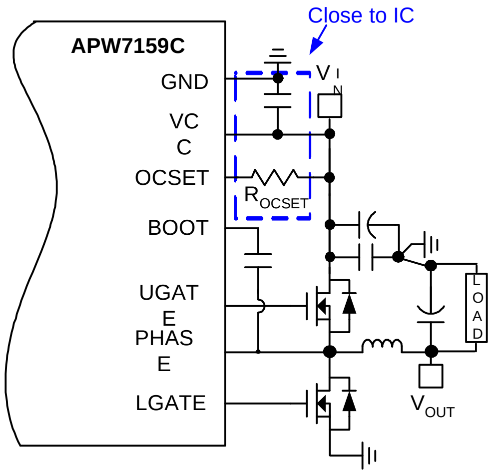
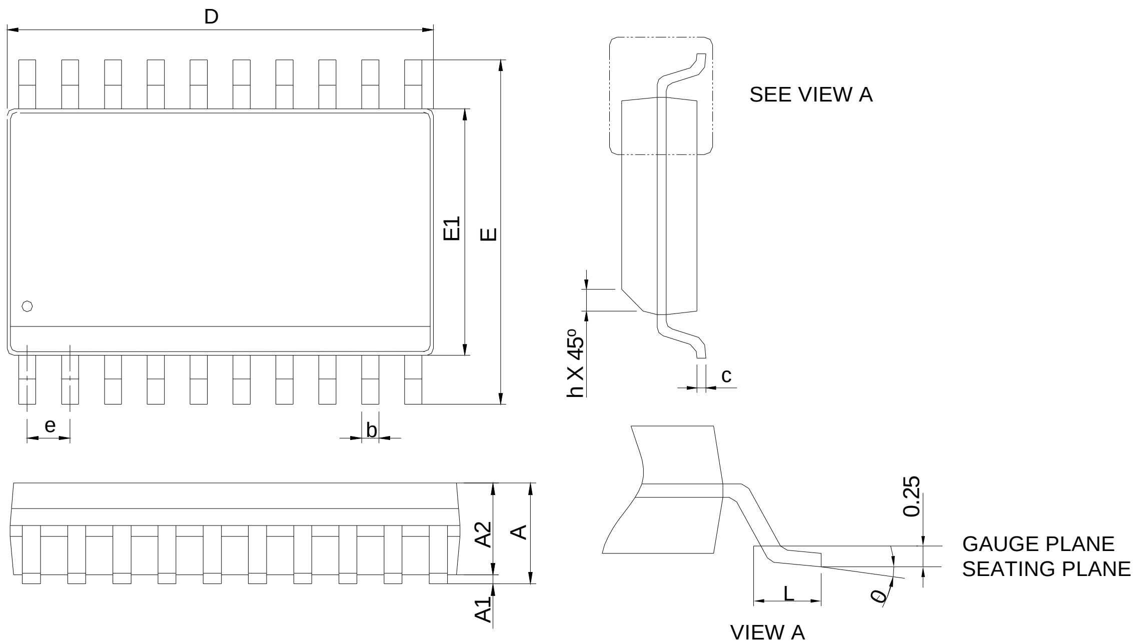


Figure 8. Layout Consideration

Package Information

SOP-20

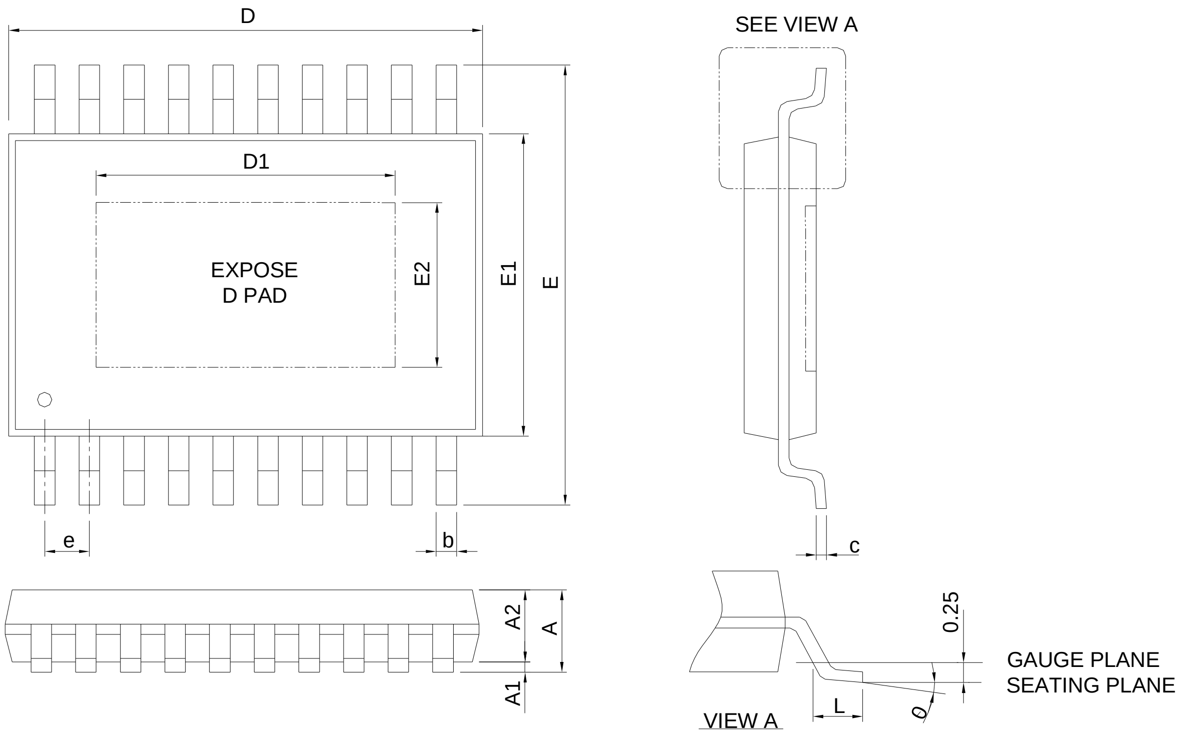


SYMBOL	SOP-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		2.65		0.104
A1	0.10	0.30	0.004	0.012
A2	2.05		0.081	
b	0.31	0.51	0.012	0.020
c	0.20	0.33	0.008	0.013
D	12.60	13.00	0.496	0.512
E	10.10	10.50	0.398	0.413
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
h	0.25	0.75	0.010	0.030
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow from JEDEC MS-013 AC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

TSSOP-20P

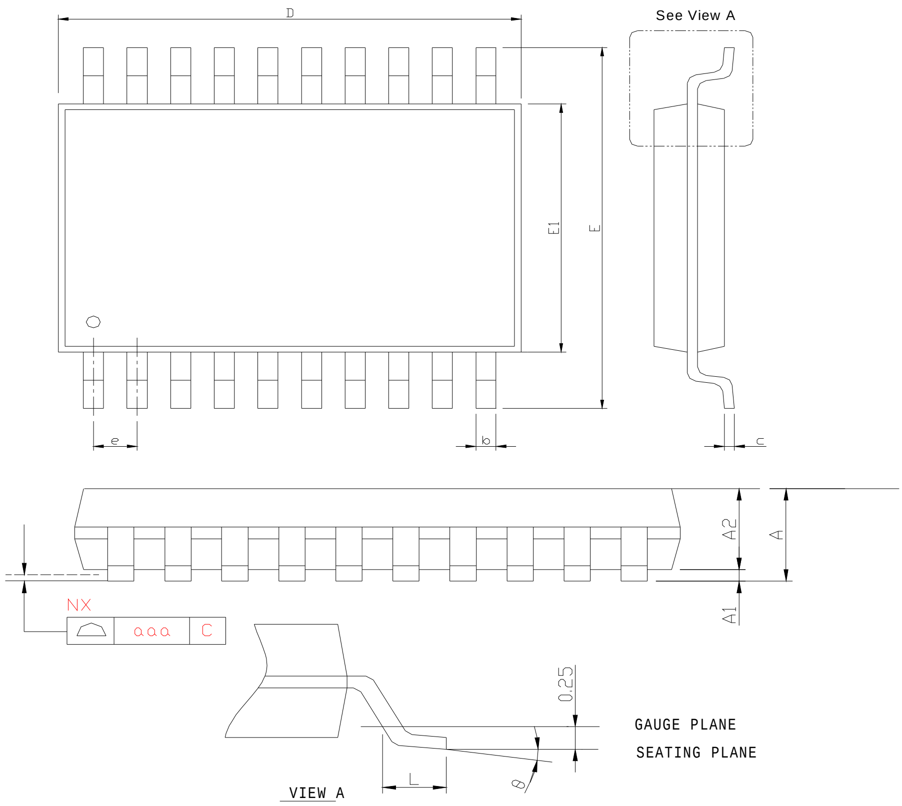


SYMBOL	TSSOP-20P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	6.40	6.60	0.252	0.260
D1	3.00	4.50	0.118	0.177
E	6.20	6.40	0.244	0.260
E1	4.30	4.50	0.169	0.177
E2	2.50	3.50	0.098	0.138
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC MO-153 ACT.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

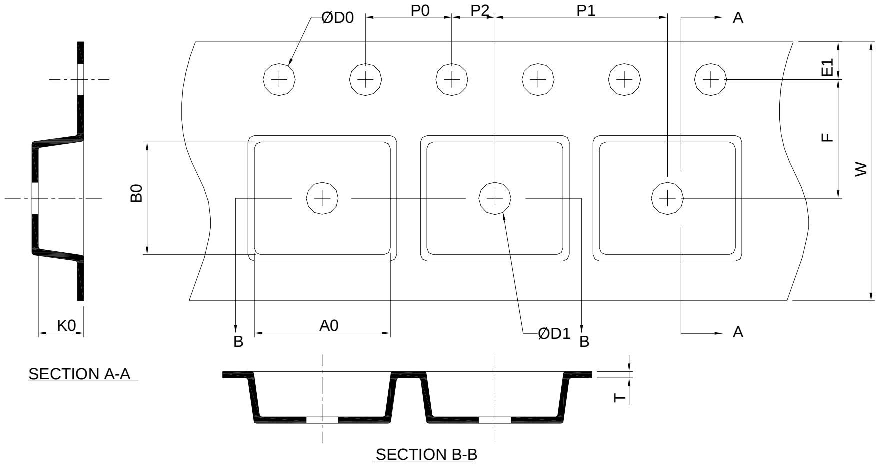
TSSOP-20P

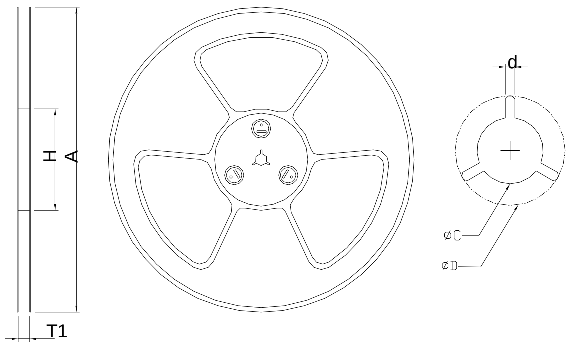


S Y M B O L	TSSOP-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	6.40	6.60	0.252	0.260
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°
aaa	0.10		0.004	

Note : 1. Followed from JEDEC MO-153 AC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
SOP-20	330.0±2.00	50 MIN.	24.40+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	24.0±0.30	1.75±0.10	11.5±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	12.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	10.9±0.20	13.3±0.20	3.1±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-20P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.30±0.05	6.9±0.20	6.90±0.20	1.60±0.20
Application	A	H	T1	C	d	D	W	E1	F
TSSOP-20	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.00±0.10	8.00±0.10	2.00±0.10	1.5+0.10 -0.00	1.5 MIN.	0.30±0.05	6.9±0.20	6.90±0.20	1.60±0.20

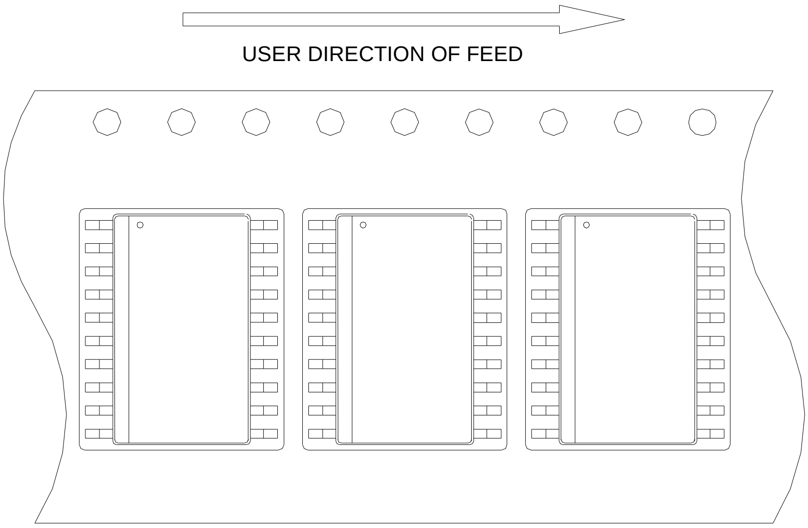
(mm)

Devices Per Unit

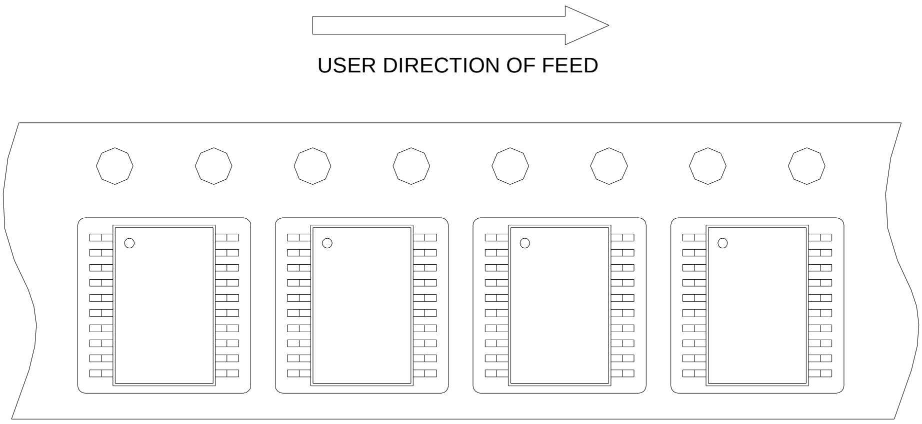
Package Type	Unit	Quantity
SOP-20	Tape & Reel	1000
TSSOP-20P	Tape & Reel	2000
TSSOP-20	Tape & Reel	2000

Taping Direction Information

SOP-20

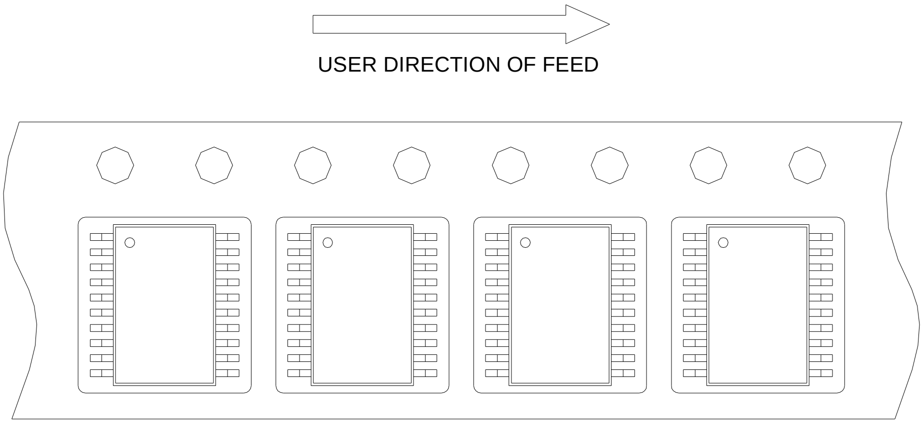


TSSOP-20P

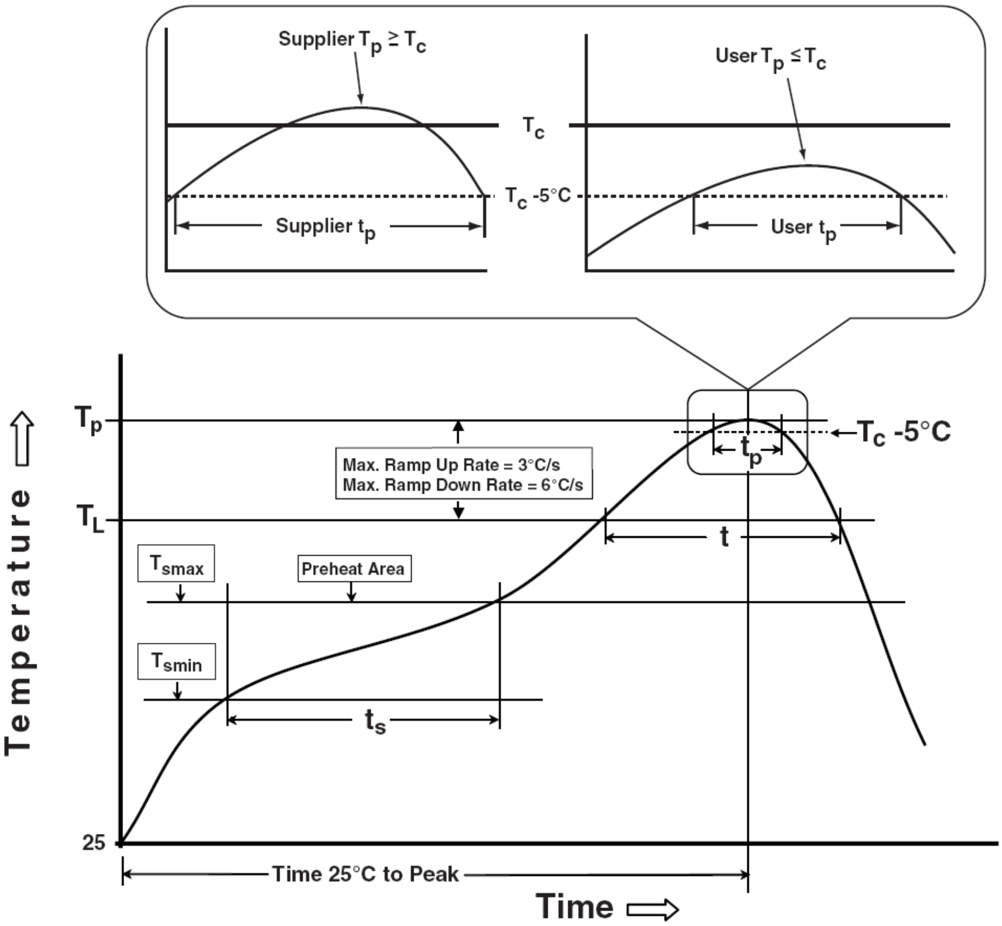


Taping Direction Information (Cont.)

TSSOP-20



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ^{3}350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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