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COMPOUND FIELD EFFECT POWER TRANSISTOR

μPA1501

N-CHANNEL POWER MOS FET ARRAY SWITCHING TYPE

DESCRIPTION

The μ PA1501 is N-channel Power MOS FET Array that built in 4 circuits and surge absorber designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Low On-state Resistance
 RDS(on) ≤ 0.42 Ω MAX. (VGS = 10 V, ID = 2 A)
 RDS(on) ≤ 0.49 Ω MAX. (VGS = 4 V, ID = 2 A)
- · Surge Absorber, built in.

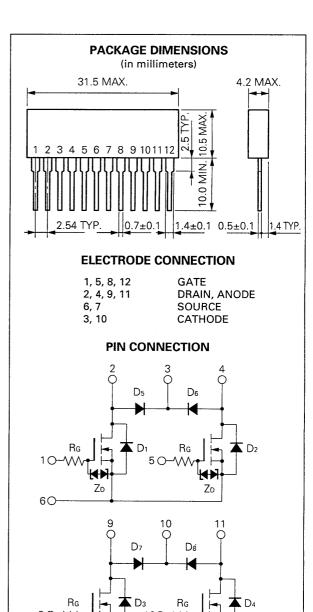
ORDERING INFORMATION

Part Number	Package	Quality Grade
μPA1501H	12-Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

Drain to Source Voltage	Voss	120	V
Gate to Source Voltage	VGSS(AC	+20, -10	V
Drain Current (DC)	ID(DC)	±3.0	A/unit
Drain Current (pulse)	ID(pulse)*	±12	A/unit
Repetitive Peak Reverse Voltage	VRRM	140	V
Diode Forward Current	IF(AV)	3.0	A/unit
Total Power Dissipation (4 circuits)	PT	4.0	W
<ta 25="" =="" °c=""></ta>			
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +15	0 °C
* PW ≦ 10 <i>u</i> s. Duty Cycle ≦ 1 %			



D₁ to D₄: Body Diode D₅ to D₈: Surge Absorber

Z_D R_G Gate to Source Protection

Gate Input Resistance

450 Ω TYP.

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ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain Leakage Current	IDSS			10	μΑ	VDS = 120 V, VGS = 0	
Gate to Source Leakage Current	Igss			±10	μΑ	$V_{GS} = ^{+20}_{-10} V$, $V_{DS} = 0$	
Gate to Source Cutoff Voltage	VGS(off)	1.0		2.5	٧	Vps = 10 V, lp = 1 mA	
Forward Transfer Admittance	yfs	2.2			S	VDS = 10 V, ID = 2 A	
Drain to Source On-state Resistance	RDS(on)1		0.42	0.55	Ω	Vgs = 10 V, lp = 2 A	
Drain to Source On-state Resistance	RDS(on)2		0.49	0.65	Ω	Vgs = 4 V, ID = 2 A	
Input Capacitance	Ciss		620		pF	V _{DS} = 10 V V _{GS} = 0 f = 1.0 MHz	
Output Capacitance	Coss		140		pF		
Reverse Transfer Capacitance	Crss		10		pF		
Turn-On Delay Time	td(on)		75		ns	ID = 2 A VGS = 10 V - VDD = 30 V RL = 15 Ω See Fig. 1	
Rise Time	tr		60		ns		
Turn-Off Delay Time	td(off)		900		ns		
Fall Time	tf		200		ns		
Total Gate Charge	QG		13		nC	Vgs = 10 V	
Gate to Source Charge	Qgs		3		nC	ID = 3 A VDD = 48 V	
Gate to Drain Charge	Qgp		2		nC	See Fig. 2	

SURGE ABSORBER (Diode, built in) 1 Unit

Repetitive Peak Reverse Current	IRRM		10	μΑ	VR = 140 V
Diode Forward Voltage	VF	1.2		٧	IF = 3 A, VGS = 0

Fig. 1 Switching Test Circuit

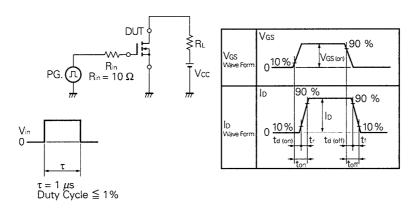
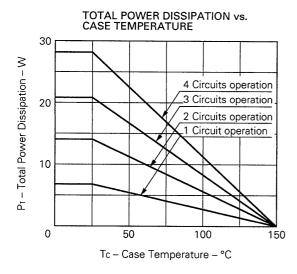
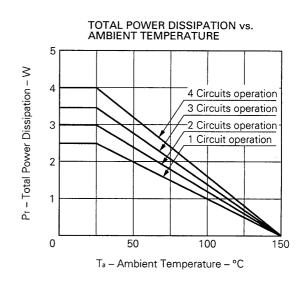
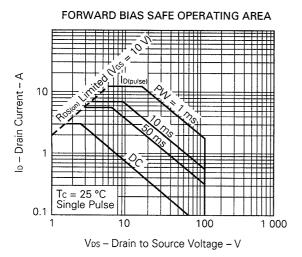


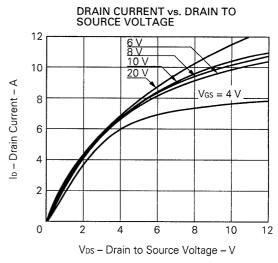
Fig. 2 Gate Charge Test Circuit

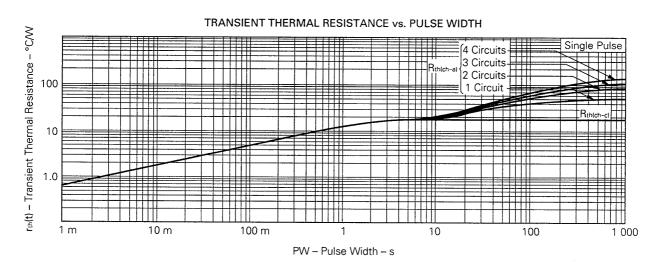
TYPICAL CHARACTERISTICS (Ta = 25 °C)

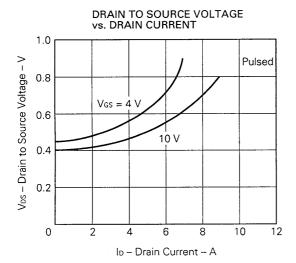




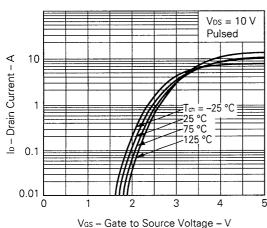




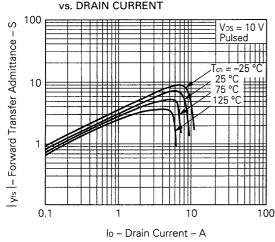




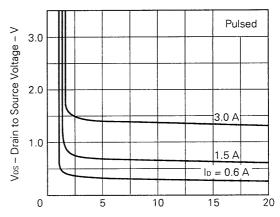
TRANSFER CHARACTERISTIC



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

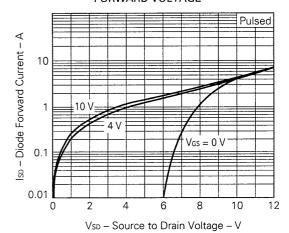


DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

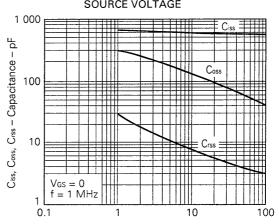


V_{GS} – Gate to Source Voltage – V

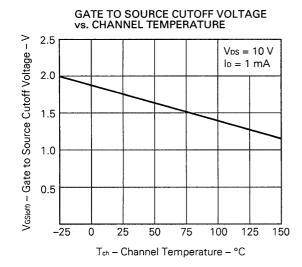
SOURCE TO DRAIN DIODE FORWARD VOLTAGE

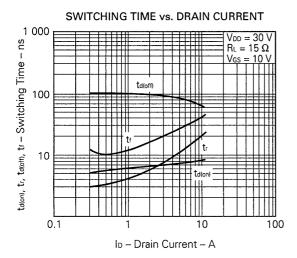


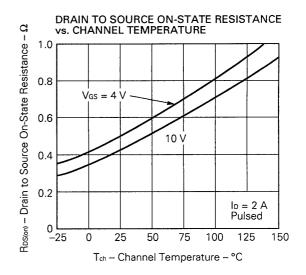
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

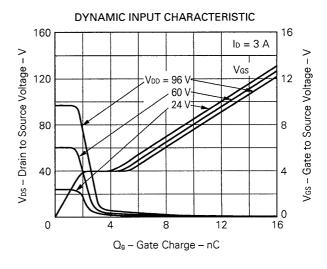


V_{DS} - Drain to Source Voltage - V









Reference

Application note name	No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Application circuit using Power MOS FET	TEB-1035

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